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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,607	10/24/2003	David N. Goldberg	10019885-1	8809

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,607	GOLDBERG ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/18/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/692,607 filed on 10/24/2003, claims 1-20 are pending.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because state that Abstract lacks narrative format and merely paraphrase claim 1. Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claims 2 and 12 are objected to because of the following informalities: these claims state "determining from a Steiner tree analysis". This limitation is not clear that what is information to be determined from a Steiner tree analysis? Applicant is advised to clarify these limitations. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1 and 11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant does not clearly describe or show (see figures 2- 4) that (as claim 1) how the step (a) could be performed more frequently then step (b) and (as claim 11) how the step (d) could be performed more frequently then step (e).

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claims 1 and 11 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Applicant's specification is not clear about (as claim1) how the step (a) could be performed more frequently then step (b) and (as claim 11) how the step (d) could be performed more frequently then step (e).

10. Claims 2-10 and 12-20 are also rejected under 35 U.S.C. 112, second paragraph, because these claims depend directly or indirectly to the claims 1 and 11.

11. For the examining purpose, Examiner interprets the limitation (as claim1) how the step (a) could be performed more frequently then step (b) and (as claim 11) how the step (d) could be performed more frequently then step (e) as broadly reasonable based on figures 2-4 and ¶0016, ¶0019, and ¶0026 in the US PG Pub (2005/0091621 A1) as it is just looping to repeat static timing analysis at early stage that estimates the path delays based on cardinality several time before performing estimate the path delay based on routing distance (wire length), if it is not resolve timing problem, then goes back static timing analysis at early stage until timing problem has been solved.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claim1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Boyle (Boyle) et al. (US 6,557,145).

14. **With respect to claim 1**, Boyle discloses a method of designing (Abstract) an application specific integrated circuit (ASIC), comprising:

(a) performing static timing analysis (figure 2, steps [108 and 113]) on versions of an ASIC design multiple times before routing (figures 7A-7B, all step performed before step 18) said ASIC design (figure 2, loop of steps [103, 105, 250, 108, and 108])

utilizing path delays that are estimated according to cardinality of fanout of nets of said ASIC design (col. 11, ll. 9-23 and col. 12, ll. 45-59); and

(b) performing static timing analysis (figure 2, step [108 and 113]) on versions of said ASIC design multiple times before routing (figures 7A-7B, all step performed before step 18) said ASIC design (figure 2, loop of steps [103, 105, 250, 108, and 108]) utilizing path delays that are calculated from estimated routing distances within a current version of said ASIC design (col. 7, ll. 10-26), wherein step (a) is performed more frequently than step (b) (see the loops from figures 1-2 and 7A-7B and see their descriptions).

15. **With respect to claim 11**, Boyle discloses A method of designing an application specific integrated circuit (ASIC), comprising:

(a) performing floor planning of an ASIC design (figure 2, step [103]);

(b) performing layout of said ASIC design (figure 2, steps [110,111, and 210]);

(c) routing said ASIC design (figure 7A-7B, step 18);

(d) performing static timing analysis (figure 2, step [108 and 113]) on versions of said ASIC design multiple times during steps (a)-(b) (figure 2, loop of steps [103, 105, 250, 108, and 108]) utilizing path delays that are estimated according to cardinality of fanout of nets of said ASIC design (col. 11, ll. 9-23 and col. 12, ll. 45-59); and

(e) performing static timing analysis (figure 2, step [108 and 113]) on versions of said ASIC design multiple times during steps (a)-(b) (figure 2, loop of steps [103, 105, 250, 108, and 108]) utilizing path delays that are calculated from estimated routing distances within a current version of said ASIC design (col. 7, ll. 10-26), wherein step

(d) is performed more frequently than step (e) (see the loops from figures 1-3 and 7A-7B and see their descriptions).

16. **With respect to claims 2 and 12**, Boyle discloses the method of claim 1 further comprising: determining from a Steiner tree analysis that said ASIC design does not satisfy a timing requirement (col. 11, ll. 53-58 and col. 17, ll. 33-55).

17. **With respect to claims 3 and 13**, Boyle discloses the method of claims 1 and 11, respectively, further comprising: flagging a circuit path of said ASIC design that does not satisfy a timing requirement (col. 2, ll. 38-42 and col. 13, ll. 50-52).

18. **With respect to claims 4 and 14**, Boyle discloses the method of claims 3 and 13, respectively further comprising: repeating at least one ASIC design process to adapt said flagged circuit path to said timing requirement (col. 2, ll. 38-47).

19. **With respect to claims 5 and 15**, Boyle discloses the method of claims 4 and 14, respectively wherein said at least one ASIC design process is logical synthesis (col. 2, ll. 41-44).

20. **With respect to claims 6 and 16**, Boyle discloses the method of claims 4 and 14, respectively wherein said repeating at least one ASIC design process includes modifying a register transfer language description (col. 1, ll. 47-50 and col. 2, ll. 41-47).

21. **With respect to claims 7 and 17**, Boyle discloses the method of claims 1 and claim 11, respectively further comprising: utilizing a static timing analysis estimated from a Steiner tree to modify a wire load model utilized to estimate timing delays associated with said cardinality of fanout of nets (col. 13, ll. 33-55).

22. **With respect to claims 8 and 18**, Boyle discloses the method of claims 7 and 17, respectively further comprising: updating a wire load table (col. 11, ll.15-22, ll. 32-52 and col. 12, ll. 6-16).

23. **With respect to claims 9 and 19**, Boyle discloses the method of claims 8 and 18, respectively wherein said wire load table comprises estimated capacitive loads of nets associated with a plurality of cardinal values of fanout (col. 12, l. 45-59).

24. **With respect to claims 10 and 20**, Boyle discloses the method of claims 1 and claim 11, respectively further comprising: routing said ASIC design (col. 2, ll. 30-34); and performing a timing analysis after performing said routing utilizing three-dimensional modeling of said ASIC design and lumped RC analysis (col. 2, ll. 35-38).

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Barnes (US PG pub 2005/0010889 A1) is performing static timing analysis from wire load. Mukherjee et al. (US 6,480,998) teaches static timing analysis based on Steiner tree.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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